Zhen Yang Journal

M1

Sunday Oct. 1 2022 150mins

meet with team go through all parts of our design

Sunday Oct. 1 2022 120mins

worked on procedure call convention,

register design

instruction design

Monday Oct. 2 2022 3hours

met with prof Robert and prof Sid to figured out some problems met but unsolved yesterday

worked on relprime assembly code

worked on relprime machine translation

worked on revised format and instruction

M2

Sunday Oct. 9 2022 5 hours

revised our design totally into an actual accumulator type

rewrote type, instruction, assembly code for relprime and gcd, design convention.

Monday Oct 10 2022 2 hours

continued to revised M1’s result a little bit

met with Josiah to explain the stuff.

write some RTL for part of our instructions.

Tuesday Oct 11 2022 3.3hours

Worked on RTL summary chart

Worked on Needed components like their input output description.

M3:

Wed Oct 17 4 hours

Design datapath and state diagram

Wed Oct 18 1 hours

Met with Ron and Josiah updated some information about datapath

Wed Oct 19 7 hours

Learn Verilog and implemented ALU, ALU-tb, mux\_5, mux\_5\_tb.

M4:

Mon Oct 24 2 hours

Finished signextender and PC Verilog

M5~M6~End:

1. Finished connecting everything altogether. And fixed all the bugs about Verilog or our machine code till the point our processor can actually do relprime.
2. Some slide stuff

Total time: quite a lot………………